APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,094	03/18/2004	Pentti Haikonen	60091.00296	5302

32294 7590 09/07/2005	EXAMINER
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	ART UNIT	PAPER NUMBER
	2819	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)
Office Action Summary		10/803,094	HAIKONEN, PENTTI
		Examiner	Art Unit
		James Cho	2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9,10,15 and 16* is/are rejected.

7)☒ Claim(s) *8 and 11-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Drawings

Figures 1-2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 11 is objected to because of the following informalities:

"the entanglement circuitry" on line 1 appears to be --the entanglement logic --, "the nodes" on line 2 appears to be --the terminals--, and "the logic elements" online 4 appears to be --the circuit elements--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7 and 9-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Wasson (US PAT No. 6,686,767).

Regarding claim 1, Figs. 2 and 4 of Wasson teaches a circuit element comprising; one or more logically entangled bi-directional terminals (output terminals of 26 in Fig. 2), wherein each bi-directional terminal can assume any one of three logical states (26 is three-state driver), which are: (a) a logical true state (logic one) (b) a logical false state (logic zero) and (c) an indefinite state (high impedance) in which state the bi-directional terminal accepts one of the logical true and logical false states as an external input from an external source (output terminals of 26 are driven by the input signals to the 26 according to control signals from control subarray coupled to 401 as shown in Fig. 4) and an entanglement logic (30 in Fig. 4 resolves conflicts from the three-state select signals by providing an enable signal; col. 2, lines 46-54) for resolving the logical state of each of the bi-directional terminals according to a predetermined set of logical entanglement rules (decoder 402 sets the rule for outputting a signal as shown in Fig. 5, i.e. first rule when ABCE =0000, the least significant driver is enabled; second rule when ABCE =1111, the most significant driver is enabled) between the bi-directional terminals.

Regarding claim 2, Figs. 2 and 4 of Wasson teaches a circuit element according to claim 1, wherein the entanglement logic is operable to perform said resolving in

response to the external input from the external source (30 perform decoding base on the control signals from control subarray in Fig. 4).

Regarding claim 3, Figs. 2 and 4 of Wasson teaches a circuit element according to claim 1, wherein the circuit element comprises several sets of logical entanglement rules (Fig. 5 shows 16 rules for enabling 16 different output drivers) and a set of additional terminals (16 output terminals of output drivers), each additional terminal accepting a logical true state or logical false state as an input (output of 26 provides signal to its output terminal), wherein the inputs to the set of additional terminals collectively determine which of several sets of logical entanglement rules are to be used for said resolving (Fig. 5).

Regarding claim 4, Figs. 2 and 4 of Wasson teaches a circuit element according to claim 1, wherein the inputs to the set of additional terminals collectively determine the logical state of one or more of the bi-directional terminals (output of 26 which is an input to its output terminal determines the state of its output terminal).

Regarding claim 5, Figs. 2 and 4 of Wasson teaches a circuit element according to claim 1, further comprising one or more circuit components, each of which has a high-impedance state, for implementing said indefinite state (tri-state driver 26 provides an high impedance state).

Regarding claim 6, Figs. 2 and 4 of Wasson teaches a network for logical

deduction, the network comprising: two or more circuit elements (first two horizontal

rows), each of which comprises: two or more logically entangled bi-directional terminals

(output terminals of five drivers, 26 in Fig. 2), wherein each bi-directional terminal can

assume any one of three logical states, which are: (a) a logical true state (logic one) (b)

a logical false state (logic zero) and (c) an indefinite state (high impedance state), in

which state the bi-directional terminal accepts one of the logical true and logical false

states as an external input from an external source (output terminals of 26 are driven by

the input signals to the 26 according to control signals from control subarray coupled to

401 as shown in Fig. 4) and an entanglement logic (30 in Fig. 4 resolves conflicts from

the three-state select signals by providing an enable signal; col. 2, lines 46-54) for

resolving the logical state of each of the bi-directional terminals according to a

predetermined set of logical entanglement rules between the bi-directional terminals;

wherein the network further comprises a set of additional terminals (output terminals of

26 on the bottom two rows in Fig. 2), each additional terminal accepting a logical true

state or logical false state as an input (26 provides logic state) wherein the inputs to the

set of additional terminals collectively determine which of several sets of logical

entanglement rules are to be used for said resolving (decoder 402 sets the rule for

outputting a signal as shown in Fig. 5, i.e. first rule when ABCE =0000, the least

significant driver is enabled; second rule when ABCE =1111, the most significant driver

is enabled).

Regarding claim 7, Figs. 2 and 4 of Wasson teaches a network according to

claim 6, further comprising an operational coupling (horizontal bus coupled to output

terminals of 26s) of each of several bi-directional terminals of one or more logic

elements to one or more additional terminals of another circuit terminal .

Regarding claim 9, Figs. 2 and 4 of Wasson teaches a network according to

claim 6, wherein each of several bi-directional terminals of one or more logic elements

is operationally coupled to one or more bi-directional terminals of another circuit

terminal (horizontal bus coupled to output terminals of 26s).

Regarding claim 10, Figs. 2 and 4 of Wasson teaches a network according to

claim 6, further comprising an interface to a data processing system for controlling and

accessing some or all of the bi- directional terminals (control signals are received from

either the unstructured array or an external device, e.g. microprocessor; col. 1, lines 55-

64).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Wasson in view of Guccione et al. (US PAT No. 6,922,665).

Regarding claims 15-16, Figs. 2 and 4 of Wasson teaches the circuit elements according to claims 1 and 6 as discussed above where PSTCC 30 being implemented with programmable logic arrays, but does not teach a computer program product including program instructions, wherein the program instructions cause a computer to simulate the circuit element. However, Guccione et al. teaches computer program for simulating a programmable logic device for the purpose of providing run time reconfiguration. It would have been obvious at the time of invention to provide a computer program for simulating the programmable logic device, PSTCC since it would provide the improved programmable logic device because of run time reconfiguration.

Allowable Subject Matter

Claims 8 and 11-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims as well as including all corrections to the claim objections stated above.

The following is a statement of reasons for the indication of allowable subject matter: one of ordinary skill in the art would not have been motivated to modify the teaching of Wasson et al. and/or Guccione et al. to further includes, among other things, the specific of the operational coupled being modifiable by external input (claim 8), and bias elements for biasing one or more of the terminals of the network toward one of the logic states (claim 11).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
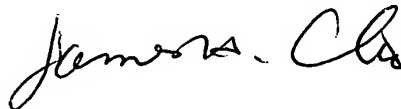
Ma et al. (US PAT No. 6,154,050) discloses a programmable logic device having an internal tristate bus with arbitration logic.

Murphy, Jr. et al. (US PAT No. 5,251,305) discloses an apparatus for preventing bus contention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

9-2-2005